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| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br><i>( Not for submission under 37 CFR 1.99)</i> | Application Number     |  | 10766761        |  |
|  | Filing Date            |  | 2004-01-28      |  |
|  | First Named Inventor   |  | Craig E. Hampel |  |
|  | Art Unit               |  | 2611            |  |
|  | Examiner Name          |  | Jia Lu          |  |
|  | Attorney Docket Number |  | RBUS 1309-1     |  |

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|------------------------|------------------|
| Application Number     | 10/766,761       |
| Filing Date            | 28 January 2004  |
| First Named Inventor   | Craig E. Hampel  |
| Group Art Unit         | 2637             |
| Examiner Name          | Jayanti K. Patel |
| Attorney Docket Number | RBUS 1309-1      |

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|  |   |    |   | Filing Date            | 28 January 2004  |
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|  |   |    |   | Group Art Unit         | 2637             |
|  |   |    |   | Examiner Name          | Jayanti K. Patel |
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| Application Number     | 10/766,761      |
| Filing Date            | 28 January 2004 |
| First Named Inventor   | Craig E. Hampel |
| Group Art Unit         | 2631            |
| Examiner Name          |                 |
| Attorney Docket Number | RBUS 1309-1     |

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| Group Art Unit         | 2631            |
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| Attorney Docket Number | RBUS 1309-1     |

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| /TW/                           | B1                    | JP                      | 02000035831A        |                                   | Nitsusan Jidosha KK                             | 08-14-1990                                       | Abstract only   |                |
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2 of

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|------------------------|-----------------|
| Application Number     | 10/766,761      |
| Filing Date            | 28 January 2004 |
| First Named Inventor   | Craig E. Hampel |
| Group Art Unit         | 2631            |
| Examiner Name          | Unassigned      |
| Attorney Docket Number | RBUS 1309-1     |

### U.S. PATENT DOCUMENTS

| Examiner Initials <sup>1</sup> | Cite No. <sup>1</sup> | U.S. Patent Document |                                   | Name of Patentee or Applicant of Cited Document | Date of Publication of Cited Document MM-DD-YYYY | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
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|                                | A27                   |                      |                                   |   |  |   |
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| Sheet  | 3 | of                 | Filing Date            | 28 January 2004 |
|  |   |                    | First Named Inventor   | Craig E. Hampel |
|  |   |                    | Group Art Unit         | 2631            |
|  |   |                    | Examiner Name          | Unassigned      |
|  |   |                    | Attorney Docket Number | RBUS 1309-1     |

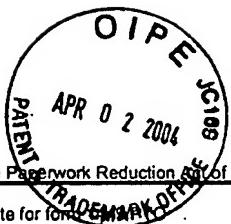
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| /TW/  | C1                    | U.S. Patent Application No. 10/278,708 filed 22 October 2002, entitled "Phase Adjustment Apparatus and Method for a Memory Device Signaling System."  |  |                |
| /TW/  | C2                    | DANIELE, N. et al., "Principle and Motivations of UWB Technology for High Data Rate WPAN Applications," SOC 2003, 4 pages.  |  |                |
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| /TW/  | C6                    | Yang, Chih-Kong Ken "Design of High-Speed Serial Links in CMOS" Technical Report No. CSL-TR-98-775, Sponsored By Center for Integrated Systems, Sun Microsystems and LSI Logic Inc. December 1998, pp. 1-182.   |  |                |
| /TW/  | C7                    | RaSer™ X Product Brief, "Highly Flexible 10 Gbps Backplane Serial Link Interface," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.   |  |                |
| /TW/  | C8                    | Yellowstone Technology Brief, "High Performance Memory Interface Technology," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.  |  |                |
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| Application Number 10/766,761   |       |
| Filing Date 28 January 2004   |       |
| First Named Inventor Craig E. Hampel  |       |
| Art Unit Unassigned   |       |
| Examiner Name Unassigned  |       |
| Attorney Docket Number RBUS 1309-1  |       |
| Sheet 1   | of 12 |

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Sheet

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of

2

Application Number

10/766,761

Filing Date

28 January 2004

First Named Inventor

Craig E. Hampel

Art Unit

Unassigned

Examiner Name

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Attorney Docket Number

RBUS 1309-1

**NON PATENT LITERATURE DOCUMENTS**

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| /TW/               | C1                    | U.S. Patent Application No. 10/278,478, Filed 22 October 2002 entitled "Timing Calibration Apparatus and Method for a Memory Device Signaling System"   |                |
| /TW/               | C2                    | Chang, Kun-Yung "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages  |                |
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| Sheet  | 1 | of | 4 | Filing Date            | 28 January 2004 (Herewith) |
|  |   |    |   | First Named Inventor   | Craig E. Hampel            |
|  |   |    |   | Group Art Unit         |                            |
|  |   |    |   | Examiner Name          |                            |
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|                       |                       | Number               | Kind Code <sup>2</sup> (if known) |   |  |   |
| /TW/                  | A1                    | 4,384,354            |                                   | Crawford et al.                                 | 05/17/1983                                       |   |
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| Filing Date  | 28 January 2004 (Herewith) |    |   |                        |             |
| First Named Inventor   | Craig E. Hampel            |    |   |                        |             |
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| <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> |   |    |   | Application Number     |                            |
| (use as many sheets as necessary)                    |   |    |   | Filing Date            | 28 January 2004 (Herewith) |
|  |   |    |   | First Named Inventor   | Craig E. Hampel            |
|  |   |    |   | Group Art Unit         |                            |
|  |   |    |   | Examiner Name          |                            |
| Sheet  | 3 | of | 4 | Attorney Docket Number | RBUS 1309-1                |

| OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS |                       |   |  |  |                |
|---|-----------------------|---|--|--|----------------|
| Examiner Initials*                                | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. |  |  | T <sup>2</sup> |
| /TW/  | C1                    | PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SDRAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.  |  |  |                |
| /TW/  | C2                    | NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.   |  |  |                |
| /TW/  | C3                    | GILLINGHAM, PETER, "SDRAM Architectural and Functional Overview," SDRAM Consortium (29 Aug 1997), 1-14.   |  |  |                |
| /TW/  | C4                    | "Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages  |  |  |                |
| /TW/  | C5                    | GILLINGHAM, PETER, "SDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39  |  |  |                |
| /TW/  | C6                    | SDRAM Inc., "400 Mb/s/pin SDRAM," Draft Advance (9 Jul 1998), 1-69.   |  |  |                |
| /TW/  | C7                    | ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."   |  |  |                |
| /TW/  | C8                    | ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."   |  |  |                |
| /TW/  | C9                    | RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages   |  |  |                |
| /TW/  | C10                   | RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages   |  |  |                |
| /TW/  | C11                   | RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages   |  |  |                |

|                    |            |                 |            |
|--------------------|------------|-----------------|------------|
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